REMARKS

Claims 1-37 are pending in the current application. In an Office Action dated April 21, 2006 ("Office Action"), the Examiner appears to have issued an obviousness-type non-statutory double-patenting rejection of claims 1-37, although the Examiner did not explicitly state those claims of the current application to which the double-patenting rejection is directed. In addition, the Examiner rejected claims 1-37 under 35 U.S.C. §102(b) as being anticipated by Brandenburg et al., U.S. Patent No. 3,742,144 ("Brandenburg"). Applicants' representative respectfully traverses both the double-patenting rejections and the 35 U.S.C. §102(b) rejections of the current claims.

Applicants' representative confesses to being completely perplexed by the Office Action. The obviousness-type non-statutory double-patenting rejection is unfounded and improper, and the cited reference, Brandenburg, is unrelated to the current application, and precedes the entire field of technology of the current invention by several decades.

First, U.S. Patent Publication No. 20050193356 was filed September 1, 2005, and is a continuation-in-part application of the current application, filed almost 2 years earlier on September 10, 2003. While it might be proper to require a terminal disclaimer in a later-filed patent application, it is improper to require a terminal disclaimer in the parent. The parent application is entitled to its full term. Moreover, the Examiner states that claims 1, 17, 34, and 36 of the current application contain every element of respective claims 5, 7, 12, 17 of the co-pending application, U.S. Patent Application Publication No. 20050193356. This statement is not true, as can be readily observed by comparing claim 1 of the current application, below, to claim 1 of U.S. Patent Publication No. 20050193356, which follows:

Current Application:

> 1. A nanoscale interconnection interface comprising:
>
> a first number of input address signal lines that carry addresses separated from one another by a first average Hamming distance;
>
> a second number of coded address signal lines; and
>
> a third number of nanowires, each nanowire addressed by one or more coded addresses comprising signals carried by the coded address signal lines and derived from an input address received on the input address signal lines, the

internal nanowire addresses separated from one another by a second average Hamming distance greater than the first average Hamming distance.

U.S. Patent Publication No. 20050193356:

1. A nanoscale interconnection interface comprising:
a number *m* of input address signal lines;
a number *n* of internal address signal lines interconnected with the *m* input address signal lines; and
a number of nanowires less than or equal to 2^k, where *k* is less than *n* and the number of nanowires is less than 2^n, each nanowire addressed by an *n*-bit internal address carried by the *n* internal address signal lines, each nanowire interconnected with one or more of the *n* internal address signal lines by resistor-like nanowire junctions, each nanowire mapped to an *n*-bit internal address, and each nanowire accessed by input of an *m*-bit external address to the *m* input address signal lines. (underline emphasis added)

Portions of the third element of claim 1 of U.S. Patent Application No. 20050193356 different from the third element of claim 1 of the current application are underlined, above, to draw the Examiner's attention to the many differences between the two claims. Claim 1 of U.S. Patent Application Publication No. 20050193356 can readily be observed to include significant limitations not present in claim 1 of the current application. That is why U.S. Patent Application Publication No. 20050193356 was filed as a continuation-in-part application--namely, to claim new, specific embodiments of nanoscale interconnection interfaces that were not claimed in the parent. In short, U.S. Patent Application Publication No. 20050193356 is both patentably distinct from the current application, and was filed almost two years after the current application. The double-patenting rejection is both unwarranted and improper.

Brandenburg is completely unrelated to the disclosure of the current application in the invention claimed by the current application. The Examiner states, in the Office Action, that "Brandenburg discloses an equivalent interconnecting or nanoscale interface." *Brandenburg does not once teach, mention, or even suggest a nanoscale interface, or anything else implemented at the nanoscale.* Nanoscale electronics had not even been imagined at the time that Brandenburg was filed, in 1971. There is not one reference in Brandenburg to nanoscale signal lines, nanowires, or anything else implemented at submicroscale dimensions. In the field of the invention, Brandenburg states that the "invention pertains to digital transmission systems and, more particularly, to a digital transmission system wherein a plurality of transmission loops are interconnected by switching stations which respond to address information, positioned within

each data message block, to selectively switch the message block to an interconnected loop." In other words, Brandenburg relates to digital telephone communication systems that use switching stations for transferring messages. In the paragraph beginning on line 14 of column 1, Brandenburg discusses connection of terminals by common carrier, switch transmission facilities. While, in 1971, such systems may have included, but likely did not include, certain microscale-electronic components, such systems did not, and could not possibly have, contained submicroscale or nanoscale circuitry. Please bear in mind that the first commercial 4-bit microprocessor was produced only in September of 1971. As the Examiner must surely know, to anticipate a claim, a cited reference must teach every element and limitation of a claim to anticipate the claim. As the Examiner most certainly knows, it is the Examiner's burden to show that a cited reference teaches every element and claim limitation. Brandenburg is completely unrelated to the current application. The current application claims a nanoscale interconnection that includes, as, for example, in the third element of claim 1, nanowires. Brandenburg neither teaches nor even suggests anything implemented at nanoscale dimensions. The Examiner has failed to meet his burden or proof.

In Applicant's representative's opinion, all of the claims remaining in the current application are clearly allowable. Favorable consideration and a Notice of Allowance are earnestly solicited.

Respectfully submitted,
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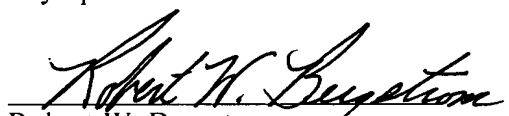

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